

U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.	Serial No.
		M-3240-3D US	Not yet assigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant	
(Use several sheets if necessary)		Coke S. Reed	
		Filing Date	Group
		Herewith	2661

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05/07/01

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>LN</i>	AA	4,814,980	3/1989	Peterson et al.	395	200.46	
<i>LN</i>	AB	4,933,836	6/1990	Tulpule et al.	395	800.12	
<i>LN</i>	AC	5,181,017	1/1993	Frey, Jr. et al.	340	825.02	
<i>LN</i>	AD	5,253,248	10/1993	Dravida et al.	370	228	
<i>LN</i>	AE	5,339,396	8/1994	Muramatsu et al.	395	312	
<i>LN</i>	AF	5,377,333	12/1994	Nakagoshi et al.	395	312	
<i>LN</i>	AG	5,471,623	11/1995	Napolitano, Jr.	395	200.03	
<i>LN</i>	AH	5,546,596	8/1996	Geist	395	200.73	
<i>LN</i>	AI	5,553,078	9/1996	Horie	370	389	
<i>LN</i>	AJ	5,577,029	11/1996	Lu et al.	379	59	
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<i>LN</i>	AL	5,606,551	2/1997	Kartalopoulos	370	406	
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<i>LN</i>	AN	5,996,020	11/1999	Reed	709	238	

Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
<i>LN</i>	AO	94 12939	6//1994	WIPO			
<i>LN</i>	AP	95 16240	6/1995	WIPO			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
<i>LN</i>	AQ	Aruna V. Ramanan, "Ultrafast Space-Time Networks for Multiprocessors", a thesis, 1993, pp. 1-170
<i>LN</i>	AR	Malek M., et al.: "The Cylindrical Banyan Multicomputer: A Reconfigurable Systolic Architecture", May 1, 1989, pp. 319-327, Parallel Computing, XP000065558
<i>LN</i>	AS	Isaac Yi-Yuan Lee et al.: "A Versatile Ring-Connected Hypercube", Jun. 1, 1994, pp. 60-67, IEEE Micro., pp. 60-67, XP000448657

Examiner	Date Considered
<i>[Signature]</i>	2/15/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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							Translation
		Document	Date	Country	Class	Subclass	Yes No
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
13N	AJ	Narashima Reddy: "I/O Embedding in Hypercubes", Aug. 19, 1988, pp. 331-338, Proceedings of the 1988 Intern'l Conf. on Parallel Processing, Pennsylvania State Univ., XP002016775					
13N	AK	Catier: "Une architecture "hypercube".", Sep. 1986, pp. 59-64, Electronique Industrielle, XP002016776					
13N	AL	Welty: "Hypercube architectures", Jun. 19, 1986, pp. 495-501, AFIPS Conference Proceedings 1986 National Computer Conference, XP002016777					
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14N	AO	Gaughan, P.T., et al.: "Adaptive Routing Protocols for Hypercube Interconnection Networks", Computer, vol. 26, No. 5, May 1, 1993, pp. 12-16, 17-23, XP000365279					
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